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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,033	ORIGASA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004 and 23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04232004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Although several discrepancies between the disclosure and drawings were noted, it is believed they all relate to oversights within the disclosure. These discrepancies are described under the following Specification section.

Specification

The disclosure is objected to because of the following informalities: Unless the reference designator --VPP-- is added to Fig. 1, it is suggested the phrase "voltage, and VPP denotes a boosted voltage" be changed to --voltage.-- on lines 20-21 of page 11, and "VPP" be deleted from line 6 on page 12. Page 14, line 16 "VENVPP3" should be --NENVPP3-- (e.g. see lines 23-25 of page 14, and the output of comparator circuit 402 shown in Fig. 4). Page 15, line 28 "606" should be --601-- to correspond to the load shown in Fig. 6, and to the description on page 16, line 4. To improve word flow, it is suggested "use" on page 16, line 6 be changed to --used--, and the term --an-- be added prior to "N-channel" on line 7 of the same page. Page 16, line 22 "VDDM" should be --VDD3-- (e.g. see Fig. 7, and related Fig. 4). Page 18, line 22 "VDD" should be --VDDM-- (e.g. see related line 19 of the same page, and Fig. 5 with respect to timing generator circuit 501). Page 19, line 12 "in put" should be the single term --input--. Page 20, line 7 "NTESTVSS" should be --NTESTVPP-- (e.g. see Fig. 9); and lines 9-10 need clarification since the output of NOR element 909 is not shown provided to the input of NOR element 910. It

is suggested lines 20-26 on page 20 be modified to more clearly indicate that each level shifting buffer 1000 provides its own respective timing signal since those lines presently appear to indicate that each buffer provides each of the four timing signals. Page 21, line 1, "102" should be --1002-- (e.g. see Fig. 10), and "1177" on line 8 should be --1117-- (e.g. see Fig. 11, and page 22, line 5). Appropriate corrections are required.

Claim Objections

Claims 2, 5-11, and 16-21 are objected to because of the following informalities: Since claim 1 already identifies the "timing generator circuit", it is suggested "a" on line 4 of claim 2 be changed to --said--. For similar reasons, "a timing signal" on line 7 of claim 2 should be changed to --said timing signal--, and "a boosted voltage" on line 12 should be --said boosted voltage--. Claim 5, line 6 should have --said-- added prior to "voltage" since the "voltage booster circuit" has already been cited twice on lines 3-5. It is suggested a comma be added after "transistor" on line 4 of claim 7 to help improve word flow (by separating "transistor" from "the gate"). Since claim 10 recites "a load", line 3 of claim 11 should have "a load" changed to --said load--. Also in claim 11, line 7 should have --said-- preceding "first" since that standard voltage was previously recited within claim 5. Claim 17, lines 11 and 14 should each have "a timing" changed to --said timing-- to correspond to the timing generator circuit and the timing signal cited on lines 5 and 4-5, respectively. Also, "a boosted" on line 19 of claim 17 should be --said boosted-- to refer back to "a boosted voltage" on line 6 of the same claim. For consistent labeling, and to minimize possible confusion, it is suggested --circuit-- be added after "pump" on line 8 of claim 18, and "a clock" be changed to --said clock-- on line 9 of the same claim. For

example, see "said charge pump circuit" and "a clock signal" on lines 24-26 of claim 17. Dependent claims carry over any objection(s) from any claim(s) upon which they depend.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Lines 1-3 of claims 1 and 17 appear to be misleading because it is not understood if the first/second voltages, and the ground voltage, are all supplied to the voltage booster power supply circuit and to the functional block circuit, or only to one of them. Therefore, clarification is requested. It is not clear how "a boosted voltage" on line 6 of claim 1 relates to "a voltage" cited on line 2 of the same claim since a functional block can use various different voltages. The use of "timing signal at a level of" on lines 7, 9-10, and 12-13 in claim 2 needs to be clarified. For example, is the timing signal constantly at the level, periodically at the level, or centered around the level? It is not understood in claim 3 how "a voltage" (line 8) relates to any of the voltages recited within claim 1. For example, is it derived from any of claim 1's voltages (e.g. see "a voltage" (line 2); "first and second voltages" (lines 2-3); and "a boosted voltage" (line 6)), or is it another distinct voltage? Claim 4, lines 5-6 "a voltage for use in said function block" is not clearly related to "a voltage" or "a boosted voltage" that are also used in the functional block as recited within claim 1. Similar to claim 3, how does "a voltage" on line 12 of claim 5 relate to the various voltages already recited within lines 2-4 of claim 5? It is not

understood if "a predetermined voltage" on line 25 of claim 5 is the same as "a predetermined voltage" recited on lines 14-15 of the same claim, or if they refer to different voltages. It is not clear in each of claims 6 (lines 5-6) and 7 (lines 8-9) how "a power supply line for providing a boosted voltage to said functional block" relates to "a voltage for use in a functional block" as recited on lines 4-5 of claim 5. For example, are these referring to the same voltage, or are they two distinct voltages used by the block? Since claim 5 recites "said second voltage being lower than said first voltage", how does claim 6's "a power supply line for providing a voltage lower than said first voltage" (lines 7-8), and claim 7's "a power supply line of voltage lower than said first voltage" (lines 11-12), relate to the second voltage? For example, are they referring to the same voltage, or to voltages that are distinct from one another? Clarification is requested with respect to how "a power supply line of said second voltage" (claim 8, line 3) and "a ground voltage line" (claim 9, line 3) each relate to "a power supply line" from claim 6, line 7. For example, do they refer to the same line, or can several different lines be connected together? It is not clear in claim 12, line 3 how "a timing signal" relates to claim 1's "a timing signal." Related to this, the phrase "converting the voltage level...to said first voltage level" on lines 3-4 of claim 12 needs clarification. For example, is the converting continuous, periodical, or does it allow the timing signal to be centered on the first voltage level? The phrase "a transistor forming said" on lines 3 and 4 of claim 16 is misleading since it can imply that the timing generator circuit and charge pump circuit are each formed by their own single, respective transistor. Therefore, it is suggested "forming said" be replaced with either --formed in-- or --within--. Similar to some previously described claims, how do claim 17's "a boosted voltage" (line 6) and "a voltage" (line 2), each being used in a functional block, relate to one another? Claim 17 's "timing signal at a

level" on lines 14, 16-17, and 19-20 have the same type of problems as described previously with respect to claim 2.

Claim 5 recites the limitation "said voltage booster circuit" in lines 3-4 with insufficient antecedent basis for this limitation in the claim. Also, how does "said voltage booster circuit" on each of lines 5, 6, 20, and 22 relate to "said voltage booster circuit" on lines 3-4, and "A voltage booster power supply circuit" on line 1? For example, it appears lines 5-6 imply "said voltage booster circuit" comprises itself, as well as a detector circuit.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujisawa et al. (Fujisawa). Fig. 15 shows a voltage booster power supply circuit that generates boosted voltage VPP, understood to be used in a functional block (e.g. see Fig. 11 and column 16, lines 18-20). The circuit is supplied with first/second voltages VDD/VDL, and ground voltage VSS, wherein second voltage VDL is lower than first voltage VDD (e.g. see column 18, lines 48-51). The output of timing generator circuit OSCILLATION CIRCUIT will be a timing signal that will be periodic, and will have a maximum (e.g. high) level corresponding to second voltage VDL. Boosted voltage VPP, understood to be used in the functional block, is generated by boosting first voltage VDD. Therefore, claim 1 is anticipated. Using Fig. 11 as an example of one type of

functional block, first voltage VDD will be used as the voltage of a power supply of block 16 when transistor Q15 is conducting, and is also the voltage of second functional block 18. Deeming the terminals coupled to voltage supplies and signals as an input/output block, one of ordinary skill in the art would understand the functional block provides/receives data from an external element, therefore claim 13 is anticipated. For example, BL/BLB is related to data that is provided and/or received. Second voltage VDL is also a voltage of a power supply provided to functional block 18,16, and it is also a voltage provided to block 16 when transistor Q16 is conducting, thus anticipating claim 14. Since the invention is related to DRAMs (e.g. see columns 1 (lines 5-7), 2 (lines 13-15), and 3 (lines 21-23)), it is also understood that the functional block comprises a dynamic random access memory, anticipating claim 15.

No claim is allowable as presently written.

Allowable Subject Matter

However, independent claims 5 and 17 would be allowable if satisfactorily rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure a voltage booster power supply circuit, supplied with first/second voltages and a ground voltage, also comprises: 1) the detector circuit's standard voltage generator circuit provides a second standard voltage by decreasing the "first voltage", and the detector circuit also has a voltage step-down circuit as recited within claim 5; or 2) level shifter circuit that outputs a timing signal, having a high level corresponding to the first voltage, to the charge pump circuit as recited within claim 17.

Also, claims 2-4, 6-12, 16, and 18-21 are would be allowable if rewritten to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the voltage booster circuit comprises the timing generator circuit, level shifter circuit, and charge pump circuit as recited within claim 2 (upon which claim 16 depends), wherein the level shifter outputs the timing signal with a high level, corresponding to the first voltage, to the charge pump circuit; 2) the detector circuit's standard voltage generator circuit provides a second standard voltage by decreasing the "first voltage" as recited within claim 3 (upon which claim 4 depends); and 3) the charge pump circuit is driven by the (converted) timing signal with respect to the first voltage level, and the substrates of a plurality of transistors within the charge pump circuit are supplied with a voltage equal to the second voltage as recited within claim 12. Claims 6-11, and 20-21 carry over the rejections of independent claim 5, and claims 18-19 carry over the rejections from independent claim 17.

Note: Although there is motivation for replacing generic type detector circuit DETECTION CIRCUIT of Fujisawa et al.'s voltage booster power supply circuit (shown in Fig. 15) with a basic known structure of a detector circuit having a voltage conversion circuit, a standard voltage generator circuit, and a comparator circuit, (e.g. see the detector circuits in Fig. 2 of Sim et al. (200, 100, and 300), and in Fig. 9 of Haraguchi et al. (161e, 161d, and 161ba, wherein those references are further described under the Prior Art section), there is no motivation to ensure the detector circuit's standard voltage generator circuit will provide a second standard voltage by decreasing the "first voltage" as recited within the applicants' claim 3. This is

because Fujisawa's DETECTION CIRCUIT is clearly shown receiving voltage VDL, which corresponds to the applicants' claimed second voltage, and that voltage is lower than first voltage VDD. Therefore, it would be assumed any circuitry within DETECTION CIRCUIT would operate from second voltage VDL, instead of first voltage VDD.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Both Haraguchi et al. and Sim et al. show/disclose known examples of a voltage booster power supply circuit, for generating boosted voltage VPP, comprising the basic elements of at least a detector circuit, a voltage booster circuit, and even if a timing generator circuit is not specifically shown, one of ordinary skill in the art would understand some type of timing generator is required to control the voltage booster circuit. For example, Sim et al. shows Vpp Generator 500 as part of the voltage booster power supply circuit in Fig. 2, but with no timing circuit shown. However, Sim et al. discloses 500 "includes a conventional oscillator and pumping circuit" on column 6, lines 16-18, wherein one of ordinary skill in the art would understand the oscillator is one known type of timing generator circuit. Using Fig. 9 of Haraguchi et al. as a specific example of a basic voltage boosting type circuit, the figure shows voltage booster power supply circuit 161 comprising detector circuit 161e,161d, 161ba-161bc and voltage booster circuit 161bd,161be. However, neither of these references shows or discloses the first/second voltages as recited, wherein: 1) a timing signal is generated with a high level corresponding to the second voltage, which independent claims 1 and 17 apparently intend to mean; or 2) the detector circuit comprises a voltage step-down circuit as recited within independent claim 5. Fig. 5 of Hagura closely corresponds to the standard voltage

generator circuit shown in the applicants' own Fig. 7, with the main difference being Hagura utilizes series coupled transistors to function as a resistance means, wherein the applicants' figure shows series coupled resistors.

The prior art reference cited on the IDS submitted on Apr 23, 2004 was reviewed and considered. Although the reference of Kondo et al. shows/discloses a voltage booster power supply circuit (e.g. see Fig. 1) for generating boosted voltage VPP; detector circuit 16; voltage booster circuit 11-13; and timing generator circuit 14, the reference does not clearly show or disclose the first/second voltages as recited, wherein: 1) a timing signal is generated according to the second voltage, which is lower than the first voltage; or) the detector circuit comprises a voltage step-down circuit.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.E

Terry L. Englund
19 July 2005

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